

- 09640113-021600
1. An apparatus in a microprocessor for executing
programmed native instructions that are provided
directly to the microprocessor via an external
instruction bus, the apparatus comprising:
instruction translation logic, configured to retrieve
macro instructions provided via the external
instruction bus, and configured to decode each of
said macro instructions into associated native
instructions for execution by the microprocessor;
and
bypass logic, coupled to said instruction translation
logic, configured to disable said instruction
translation logic, and configured to provide the
programmed native instructions for execution by
the microprocessor, thereby bypassing said
instruction translation logic.
2. The apparatus as recited in claim 1, wherein the
programmed native instructions are provided from a
memory to the external instruction bus.
3. The apparatus as recited in claim 1, wherein execution
of a native branch macro instruction causes the
microprocessor to transfer program control to the
programmed native instructions.

Pub A3

1 4. The apparatus as recited in claim 3, wherein said
2 bypass logic comprises:
3 mode detection logic, configured to detect said native
4 branch macro instruction within a macro
5 instruction sequence that is provided to said
6 instruction translation logic, wherein, upon
7 detection of said native branch macro instruction,
8 said mode detection logic directs said instruction
9 translation logic to cease decoding said macro
10 instruction sequence following decoding of said
11 native branch macro instruction.

1 5. The apparatus as recited in claim 4, wherein, said
2 instruction translation logic decodes said native
3 branch macro instruction into a native branch native
4 instruction, and wherein said native branch native
5 instruction directs the microprocessor to transfer
6 program control to a native branch target address.

1 6. The apparatus as recited in claim 5, where said native
2 branch target address is provided in an architectural
3 register.

Pub#3
1 7. The apparatus as recited in claim 4, wherein said
2 bypass logic further comprises:
3 a native instruction router, coupled to said mode
4 detection logic, configured to receive the
5 programmed native instructions, and configured to
6 route the programmed native instructions to a
7 native instruction bus.

009T80"8T04960
1 8. The apparatus as recited in claim 4, wherein, said mode
2 detection logic is also configured to detect a native
3 branch return macro instruction, said native branch
4 return macro instruction following the programmed
5 native instructions, wherein, upon detection of said
6 native branch return macro instruction, said mode
7 detection logic directs said instruction translation
8 logic to resume decoding said macro instruction
9 sequence.

1 9. The apparatus as recited in claim 8, wherein said
2 instruction translation logic decodes said native
3 branch return macro instruction into a native branch
4 return native instruction, and wherein said native
5 branch return native instruction directs the
6 microprocessor to transfer program control to a return
7 address.

Sub A3

1 10. The apparatus as recited in claim 9, wherein said
2 return address designates a next macro instruction,
3 said next macro instruction being within said macro
4 instruction sequence and following said native branch
5 macro instruction.

1 11. An apparatus, for allowing a micro instruction to be
2 directly provided from an external instruction bus to
3 execution logic within a pipeline microprocessor, the
4 apparatus comprising:
5 a translator, for receiving macro instructions from a
6 macro instruction bus, and for translating each of
7 said macro instructions into associated micro
8 instructions, said associated micro instructions
9 being provided to the execution logic via a micro
10 instruction bus; and
11 bypass logic, coupled to said translator, for routing
12 the micro instruction to the execution logic, said
13 bypass logic comprising:
14 a mode detector, for detecting a native branch
15 macro instruction, and for directing that
16 said translator cease instruction
17 translation; and
18 native instruction routing logic, coupled to said
19 mode detector, for receiving said micro

Sub A3
20 instruction from said macro instruction bus,
21 and for providing said micro instruction to
22 said micro instruction bus, thereby
23 circumventing said translator.

1 12. The apparatus as recited in claim 11, wherein the
2 external instruction bus typically provides said macro
3 instructions to the microprocessor.

1 13. The apparatus as recited in claim 11, wherein the
2 execution logic executes said native branch macro
3 instruction by transferring program control to a memory
4 address containing the micro instruction.

1 14. The apparatus as recited in claim 13, wherein said
2 memory address is provided in an architectural
3 register.

1 15. The apparatus as recited in claim 11, wherein, said
2 mode detector is configured to detect a native branch
3 return macro instruction, wherein, upon detection of
4 said native branch return macro instruction, said mode
5 detection logic directs said translator to resume
6 instruction translation.

1 16. The apparatus as recited in claim 15, wherein the
2 execution logic executes said native branch return

DUBA 3

3 macro instruction by transferring program control to a
4 return memory address.

1 17. The apparatus as recited in claim 16, wherein said
2 return memory address contains a next macro
3 instruction.

1 18. A microprocessor for executing micro instructions
2 directly from memory, the microprocessor comprising:
3 translation logic, for receiving macro instructions
4 from the memory, and for decoding said macro
5 instructions into corresponding micro instructions
6 for execution by the microprocessor;

7 mode detection logic, coupled to said translation
8 logic, for detecting bypass macro instructions,
9 and for directing the microprocessor to execute
10 the micro instructions directly from the memory
11 rather than via said translation logic, said
12 bypass macro instructions comprising:

13 a native branch macro instruction, directing that
14 program control be transferred to a target
15 address; and

16 a native branch return macro instruction,
17 directing that program control be transferred
18 to a return address; and

Sub A3

19 an instruction router, coupled to said mode detection
 20 logic, for receiving the micro instructions, and
 21 for routing the micro instructions to execution
 22 logic, thereby bypassing said translation logic.

1 19. The apparatus as recited in claim 18, wherein said mode
 2 detection logic, upon execution of said native branch
 3 macro instruction, directs said translation logic to
 4 cease decoding said macro instructions.

1 20. The apparatus as recited in claim 18, wherein said
 2 target address designates a location in the memory
 3 within which a first one of the micro instructions
 4 resides.

1 21. The apparatus as recited in claim 20, where said target
 2 address is provided in an architectural register.

1 22. The apparatus as recited in claim 18, wherein said
 2 instruction router routes the micro instructions from a
 3 macro instruction bus to a micro instruction bus.

1 23. The apparatus as recited in claim 18, wherein said mode
 2 detection logic, upon execution of said native branch
 3 return macro instruction, directs said translation
 4 logic to resume decoding said macro instructions.

Sub A3

1 24. The apparatus as recited in claim 23, wherein said
2 return address designates a next macro instruction,
3 said next macro instruction being one of said macro
4 instructions.

003T30" 8T T04960